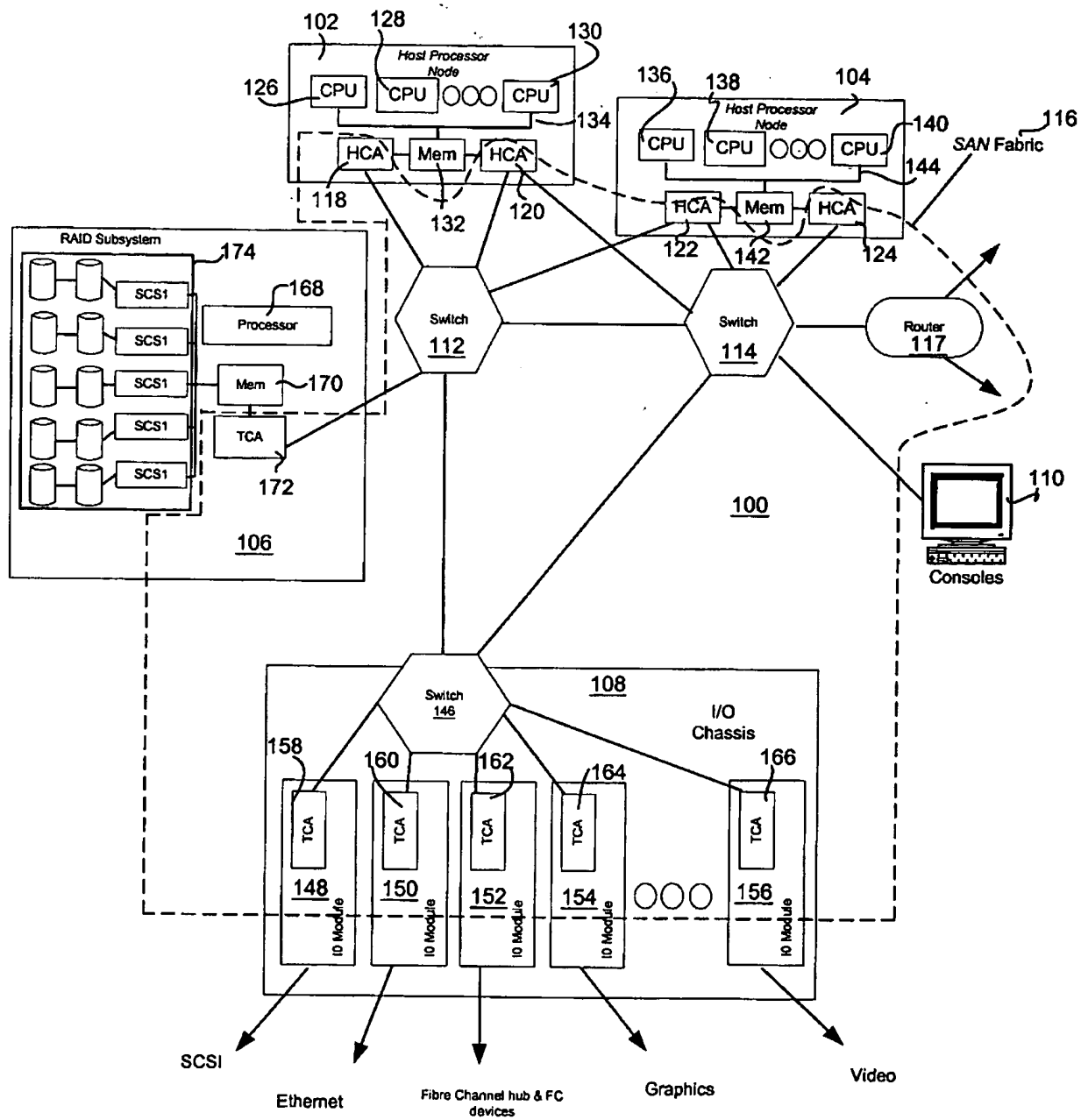


FF40965243305

Figure 1

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The diagram illustrates the architecture of a Host Processor Node 200. At the top, a horizontal bar represents the **Host Processor Node**, which contains four **Consumer** components: **Consumer 202**, **Consumer 204**, **Consumer 206**, and **Consumer 208**. These consumers are connected to a central **Message & Data Service 224**. Below this, a dashed line labeled **Verbs** separates the Host Processor Node from the Channel Adapters. On the left, a **Channel Adapter (endnode) 210** is connected to **Port 214** and **Port 216**. On the right, a **Channel Adapter (endnode) 212** is connected to **Port 218** and **Port 220**. The entire system is labeled **200** at the bottom.

Figure 2

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FIG. 3

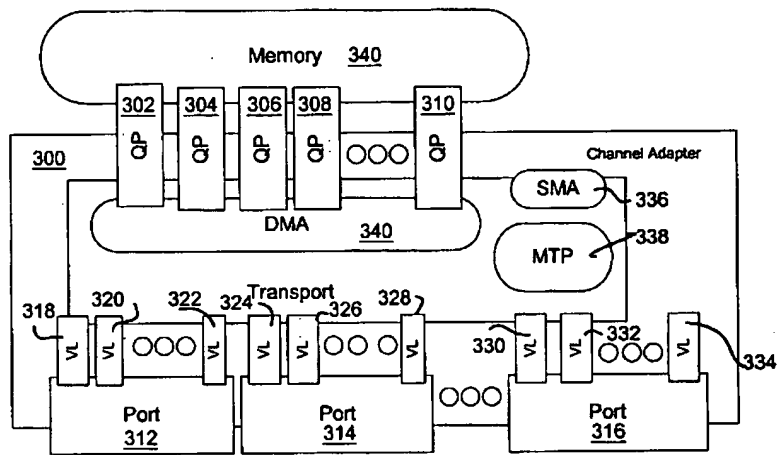


Figure 3

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Figure 4

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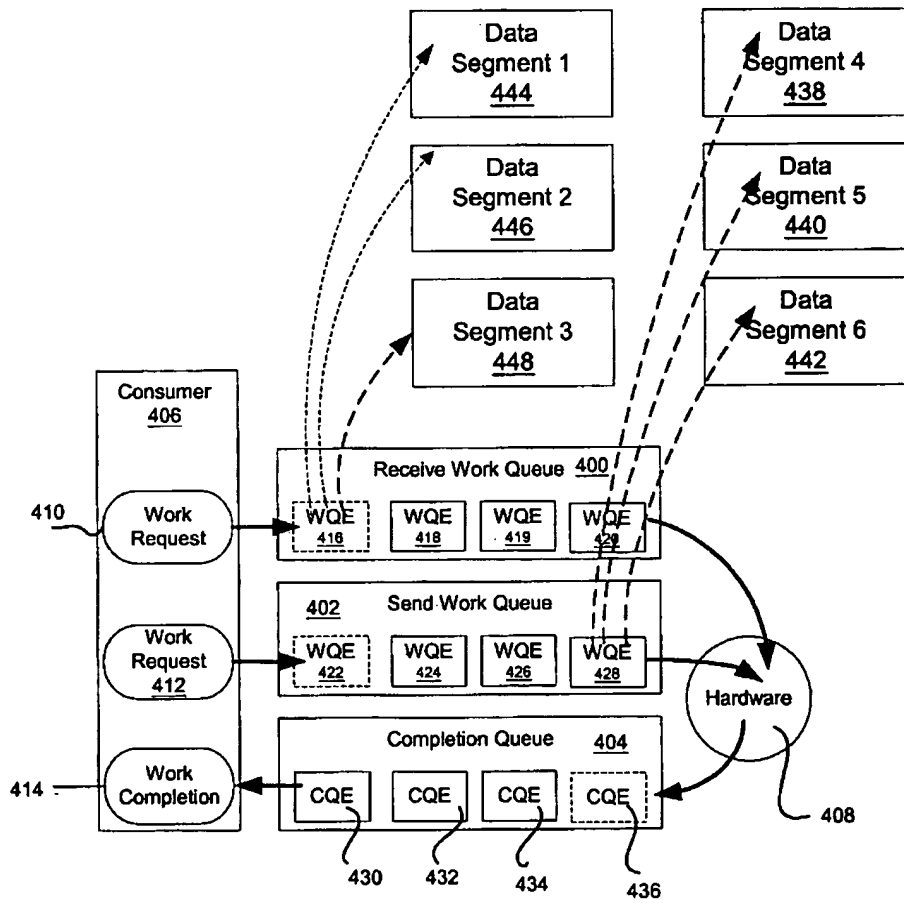


Figure 5

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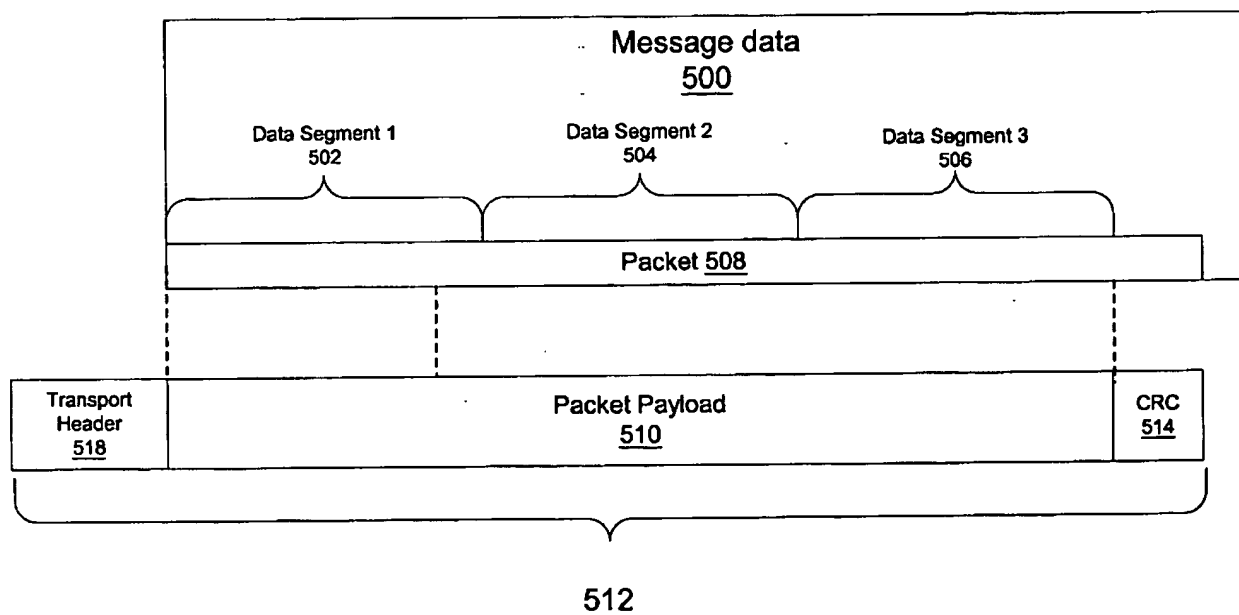


Figure 6

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bytes				
0-24	MAD Header			
24	SA_Key			
28				
32	SM_Key			
36				
40	Segment Number			
44	Payload Length			
48	Fragment Flag	Edit Modifier	Window	
52	EndRID			
56	ComponentMask			
60				
64	Admin Data (192 bytes)			
...				
252				

602

604

608

606

600

602

604

608

606

00587-0110
TOTFO 625250

Figure 7

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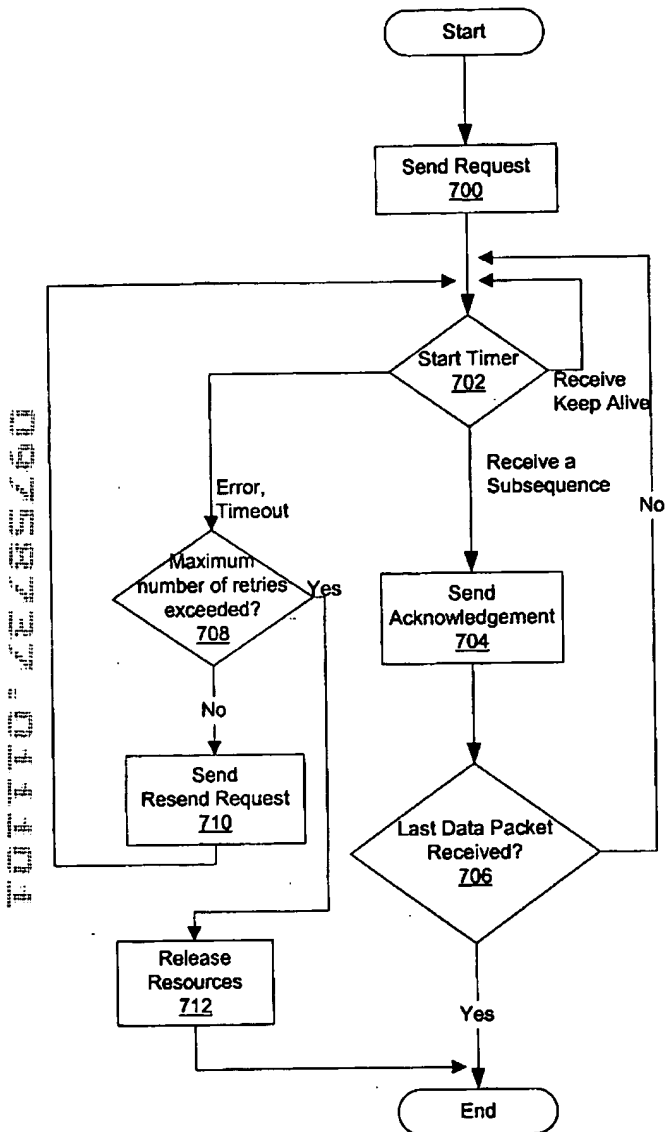


Figure 8

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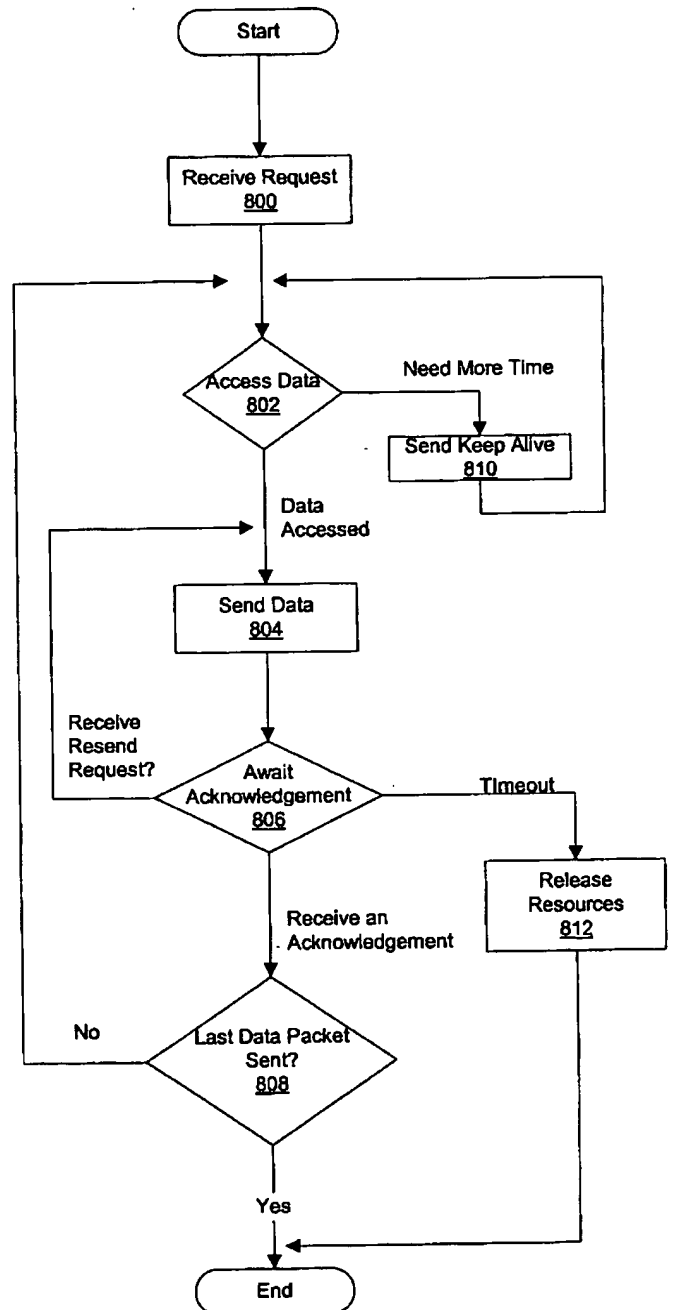


Figure 10

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FIG. 10

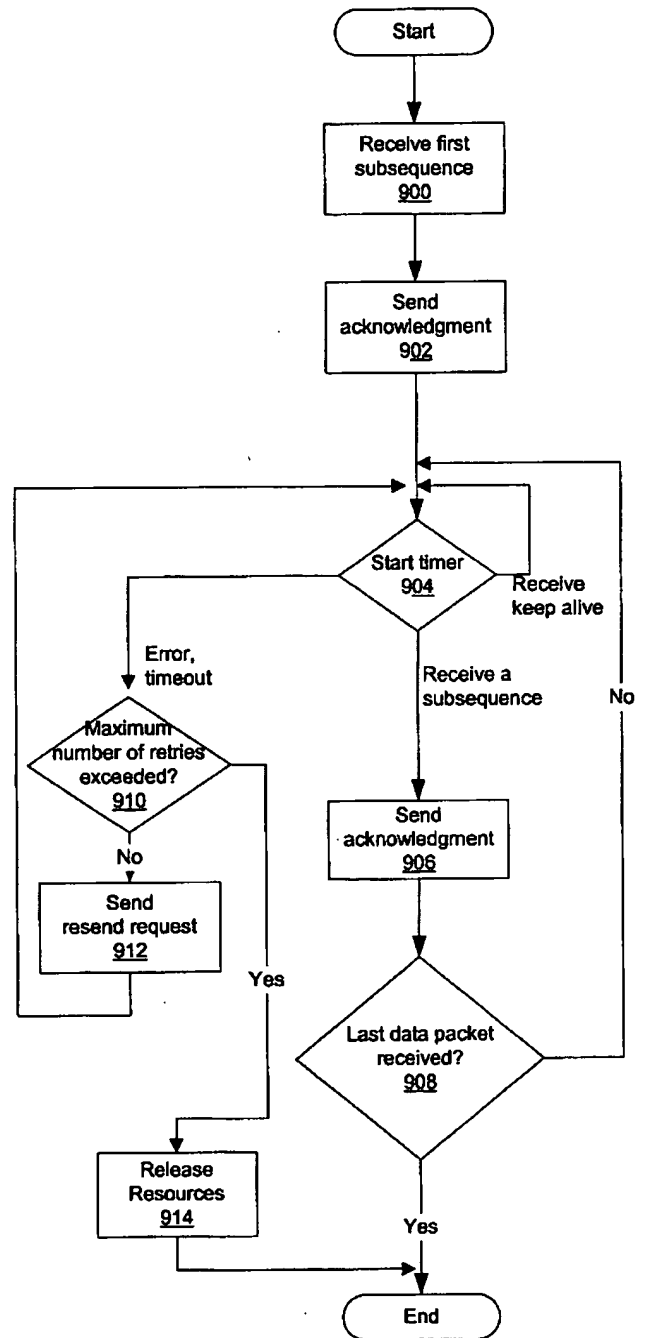
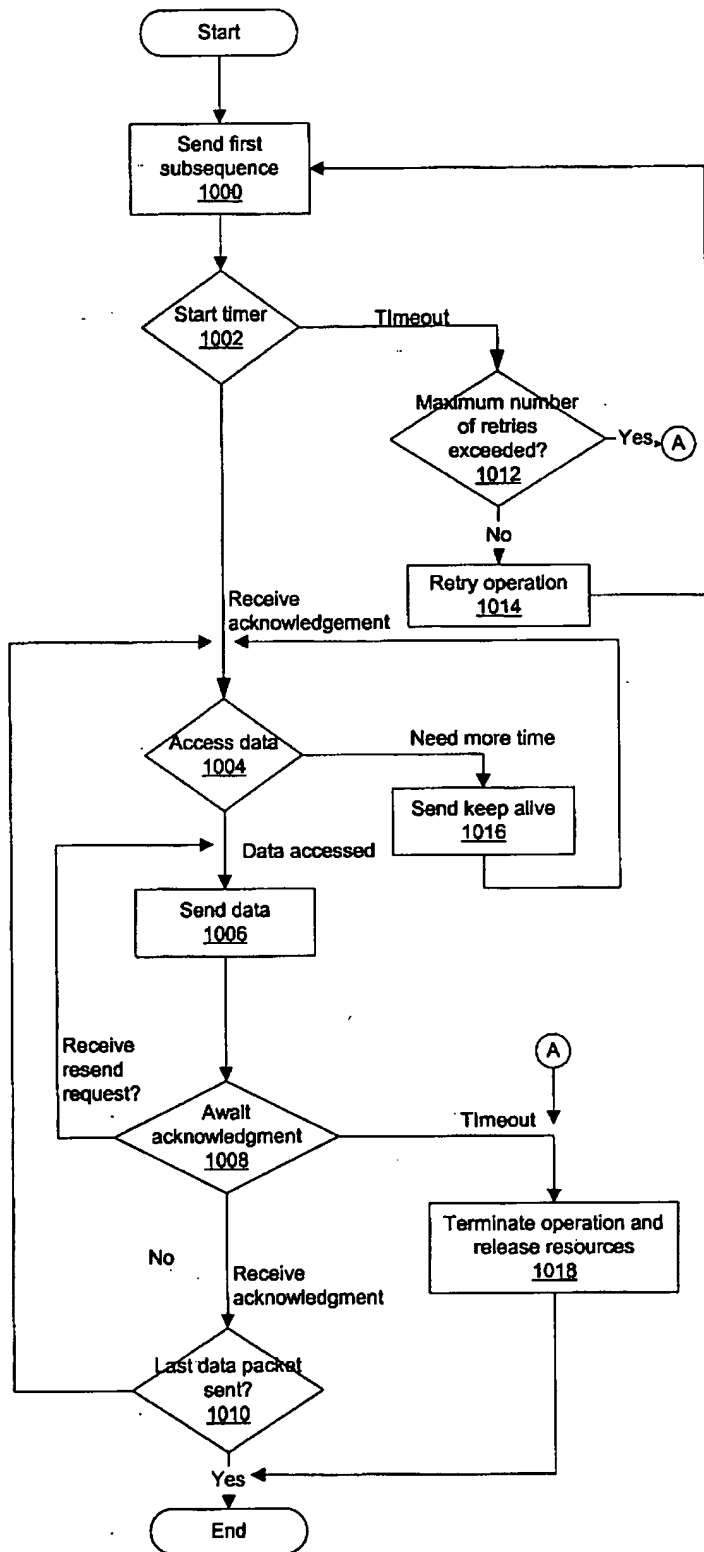


Figure 9

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